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SiC Power JFETs

Understanding and Driving these devices for maximum benefit

A white paper written by Bose Research Private Limited in collaboration with Norwegian University Of Science And Technology

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Acknowledgements

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Summary

With the commercial availability of normally-off three-terminal SiC VJFETs, their acceptance is expected to grow significantly in consideration to their excellent low switching loss characteristics, high temperature operation and high voltage rating capabilities. This paper investigates the influence of the gate drive on the switching characteristics of the device and highlights design strategies for driving them.

The superior features of wide bandgap semiconductor materials e.g. SiC and GaN over the conventionally used materials i.e. Si and GaAs allow for higher performance power electronic devices. Nowadays, SiC has the highest market share among other wide bandgap materials. SiC devices have high temperature stability [1], high thermal conductivity and high breakdown voltage allowing fast switching speed and low on-state resistance [2]. This also allows for realization of highly compact power converters, which is in demand today.

Nowadays, two classes of SiC power electronic devices are commercially available, namely Schottky diodes and field effect transistors. The first commercially available SiC power devices were SiC Schottky diodes. They were introduced by Infineon in 2001, and now are available from several manufacturers, including Infineon, Cree, IXYS, Microsemi, and STMicroelectronics, etc. Thus the SiC Schottky diode has been in the market for some years now and is widely used today in continuous conduction mode boost power factor correction converters to minimize switching losses and improve efficiency. The high voltage ratings to 1200 V and the near zero reverse recovery time of these devices, make them excellent choices for many other hard switching applications too [3].

Similarly one of the most successful and promising devices to replace Si-MOSFET and IGBT is the normally-off vertical JFET. SiC controllable switching devices are available as engineering samples such as JFETs from SiCED and SemiSouth, MOSFETs from Cree, and BJTs from Cree and TranSiC.

SiC active switches feature higher breakdown voltage, lower on-state resistance, as well as better high-temperature operation capability without sacrificing the switching speed, all of which make them very potential in the high-power, high-voltage, high-frequency and high-density applications. However methods of driving these devices is different from the Si-MOSFET or the BJT. Thus the acceptance of this type of devices depends on the understanding of its switching behaviour and the ability to design a proper driving circuit. This paper investigates the switching and drive characteristics of the SiC JFET, and a drive circuit is proposed. The circuit is tested and various experimental observations are recorded. Based on these measurements, a deeper practical insight to the device is documented.

1. SIC ENHANCEMENT –MODE NORMALLY OFF JFET

A. Device Description and Gate Requirements

Power electronic converter designers prefer normally-off transistors over normally-on types. Enhancement-mode normally-off JFET combines this feature with a voltage controlled gate. This makes it a potential candidate to replace the Si-MOSFET and IGBT. However, SiC JFET device switching behaviour is not yet thoroughly understood. Fig. 1 shows the equivalent schematic model for a JFET [4]. At the gate-source junction, a variable capacitance appears which resembles a classical MOSFET's gate-source capacitance but has a lower value in comparison to a MOSFET. A p-n diode also appears at the gate-source junction, just like that of a BJT. This requires the gate driver to deliver a dynamic charge to the gate capacitance during the turn-on and the fast removal of this charge to ensure a fast turn-off process. The other crucial gate requirement is to maintain the gate-source diode on by keeping it forward biased during the on time. The drive voltage must thus be higher than a SiC pn diode's typical built-in potential of around 3 V at 25 ^{o}C for typical doping concentrations. The gate driver circuit should maintain the diode forward current (I_{GS}) during the on period.

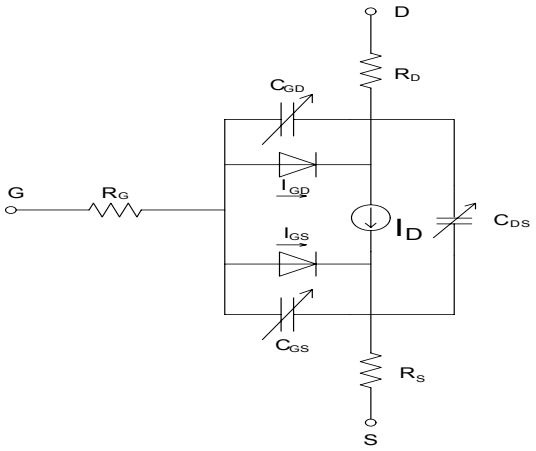

Fig. 1. Schematic model of JFET

B. ***Modelling of Gate-source Diode***

Modelling of current-voltage characteristic of the gate-source diode was done in order to estimate gate current requirement at different temperatures. A simplified diode model, proposed in [4], is used. Fig. 2 shows the simulated I-V characteristic of this diode. By keeping a voltage of 3 V at gate-source, as recommended in datasheets a minimum gate current of I_{GS} = 100 mA should be supplied to the gate when the junction temperature is 25 ^{o}C. This current raises to I_{GS} = 500 mA for T_J =175 ^{o}C.

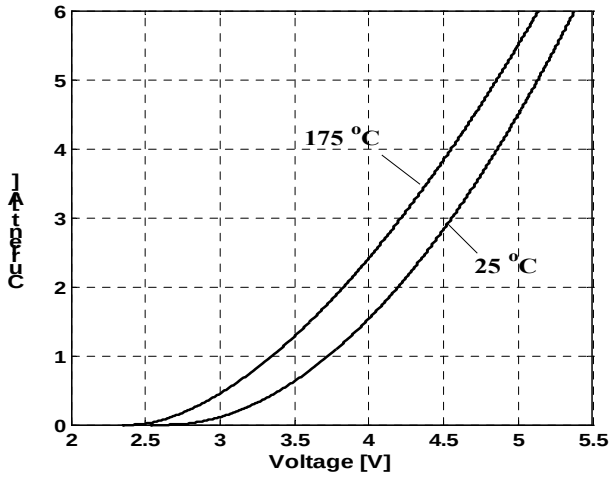

Fig. 2. Simulated I-V characteristics of gate-source diode

Diode threshold voltage is thus a temperature dependant parameter.

The higher the junction temperature the lower the voltage needed for the diode to start conducting.

2. DEVICE PHYSICS

With zero voltage at gate-source junction, the JFET channel is totally pinched off by overlapped depletion regions formed by two adjacent gate junctions. Almost no current flows between the drain and source, device output terminals shows high resistance. Applying forward bias voltage across gate-source PiN junction, depletion region width shrinks down and thus conductive channel between drain and source is formed. At relatively low VDS, injected carriers through device gate increases minority carrier concentration within this channel resulting in conductivity modulation. The device voltage-current characteristic is linear during this phase with low on-state resistance. The distribution of these minority carriers at low VDS covers the conductive channel i.e. source to drain region. However, as the VDS increases, this distribution tends to be closer to source region rather than drain, while electric field builds up. At such moderate drain voltage i.e. second phase, carriers are mainly drifted by the electric field and no conductivity modulation occurs while device resistance increases. With higher drain voltage the developed electric field reaches a critical value causing carriers to move in saturated drift velocity and thus causing current to saturate. The third conductive phase shows no increase in drain current with VDS increase. The transport of drift carriers is apparently limited by the saturation velocity. The level of saturation current here is also a function of the gate voltage, the higher the gate voltage the higher the saturation current. This is due to wider conductive channel i.e. higher conductivity, at higher gate voltage. However, no further increase in drain current results after applying a certain gate voltage value. Permanent destruction of device gate occurs at high gate voltages results due excessive flow of current through gate-source diode i.e. I_{GS}. Simulation results in Fig. 2 can be utilized to estimate current flow at different gate voltages. For the tested JFET, which is described below, gate voltage of 3 V is recommended.

3. GATE DRIVE DESIGN

A SJEC120R100 enhancement-mode JFET from Semisouth USA was selected [5]. It is a 1200 V device with $R_{DS(ON)}$ of 100 mΩ, C_{iss} = 670 pF, C_{rss} = 97 pF and C_{oss} = 103 pF. A standard NPN/PNP totem pole driver was used to drive the device and the detailed schematic design is given in Fig.3. During turn-on, R1

sets the I_{GS} to approximately 140 mA while R2/C1 provides a peak gate charging current about 0.63 A and thus aid in providing a faster turn-on. Device turn-off is provided by D1 while R2/C1 generates a negative voltage to discharge the gate capacitances and thus aid in providing a faster turn-off. A good gate drive design [6] [7] is helpful is achieving excellent switching characteristics [8] for the SiC JFET.

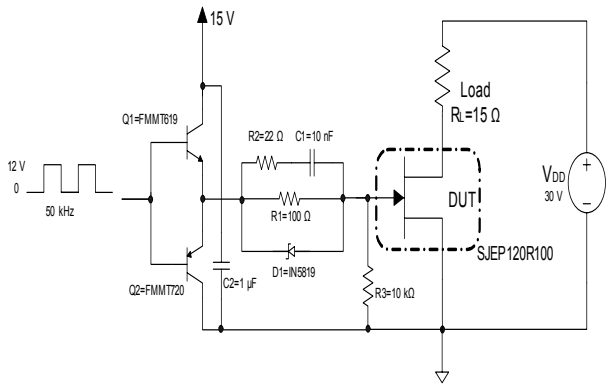

Fig. 3. A schematic diagram of the proposed driver circuit

4. EXPERIMENTAL RESULTS

The waveforms in Fig. 4a shows the switching behaviour of the SiC JEFT without the speed up capacitor C1. The figure shows a full cycle switching with approximately 50 kHz switching frequency. Channel 1 shows the totem pole driver output, Channel 2 shows the JFET gate drive voltage across R3 while Channel 3 shows the switching waveform across the drain-source of the device. An improvement both in the turn-on and turn-off time can be seen. Fig. 4b shows these waveforms with the speed up capacitor C1.

The waveforms in Fig. 5a (shown on the next page) show the turn-on behaviour of the SiC JEFT without the speed up capacitor C1. Here too, Channel 1 shows the totem pole driver output, Channel 2 shows the JFET gate drive voltage across R3 while Channel 3 shows the switching waveform across the drain-source of the device. Fig. 5b (shown on the next page) shows these waveforms with the speed up capacitor C1. It can be observed that there is a significant improvement in the turn-on switching speed by over a 100 ns with the speed up capacitor.

The waveforms in Fig. 6a (shown on the next page) show the turn-off behaviour of the SiC JEFT without the speed up capacitor C1. Here too, Channel 1 shows the totem pole driver output, Channel 2 shows the JFET gate drive voltage across R3 while Channel 3 shows the switching waveform across the drain-source of the device. Fig. 6b (shown on the next page) shows these waveforms with the speed up capacitor C1. It can be observed that the turn-off behaviour is significantly improved by over a 500 ns with the speed up capacitor.

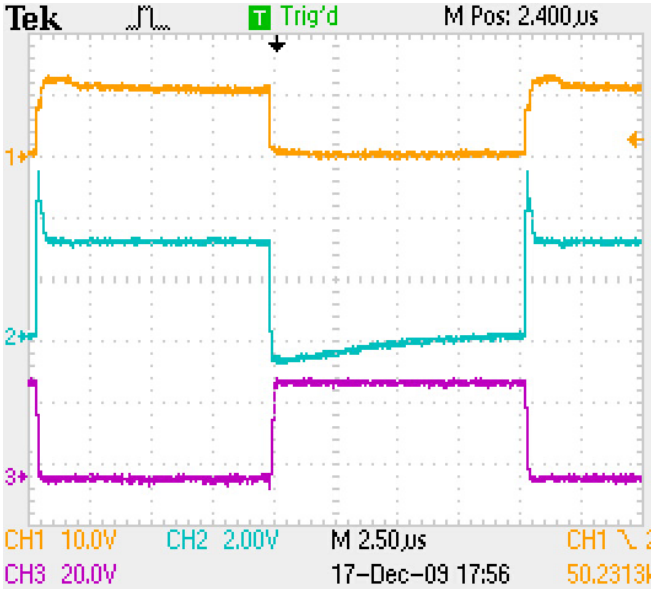

Fig. 4a. A Full switching cycle of power JFET with direct driver.

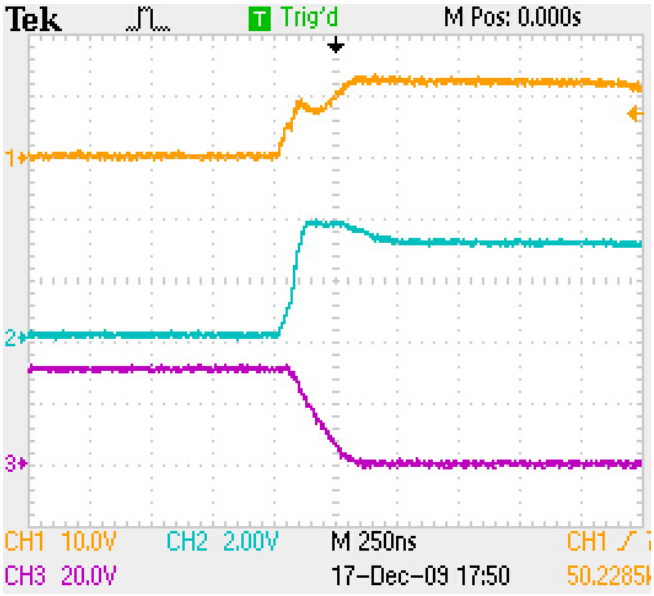

Fig. 4b. A Full switching cycle of power JFET with a 10 nF speed up capacitor.

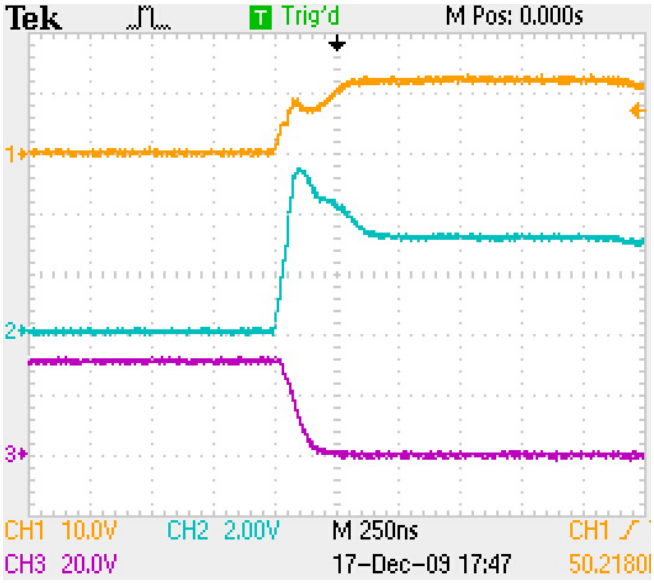

Fig. 5a. Turn-on waveforms with the device directly connected to a totem pole driver.

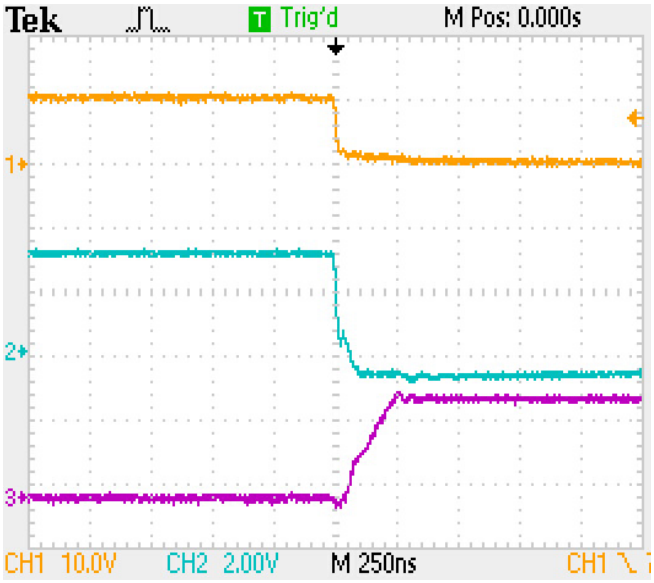

Fig. 6a. Turn-off waveforms with the device directly connected to a totem pole driver.

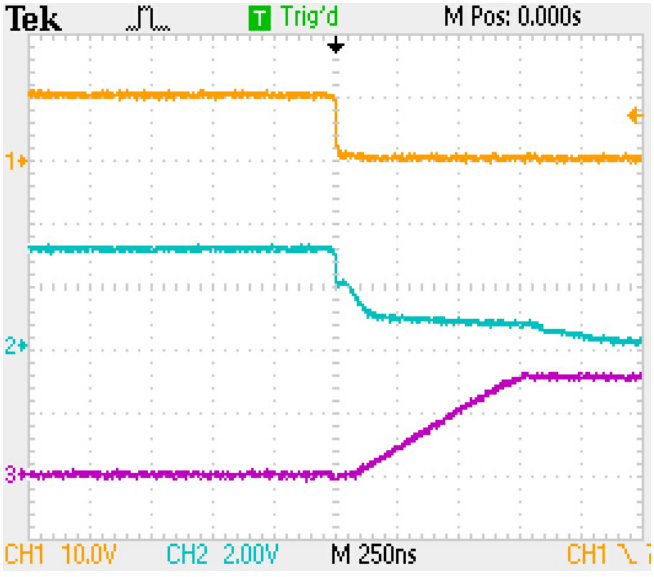

Fig. 5b. Turn-on waveforms with the device connected to a 10 nF speed up capacitor.

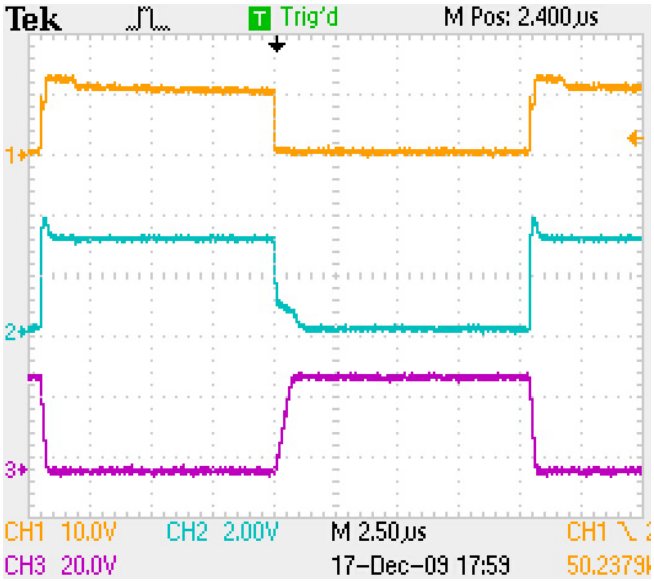

Fig. 6b. Turn-off waveforms with the device connected to a 10 nF speed up capacitor.

The waveforms in Fig. 7a show the influence of the Miller capacitance on turn-on behaviour of the SiC JEFT with the speed up capacitor C1. Channel 2 shows the JFET gate drive voltage across R3 while Channel 3 shows the switching waveform across the drain-source of the device. The Miller plateau was observed to be about 13 ns during the turn-on. The waveform in Fig. 7b shows the influence of the Miller capacitance on turn-off behaviour of the SiC JEFT with the speed up capacitor C1. Channel 2 shows the JFET gate drive voltage across R3 while Channel 3 shows the switching waveform across the drain-source of the device. The Miller plateau was observed to be about 19 ns during the turn-off. The significantly small capacitance of the JFET when compared to MOSFET explains the small Miller plateau.

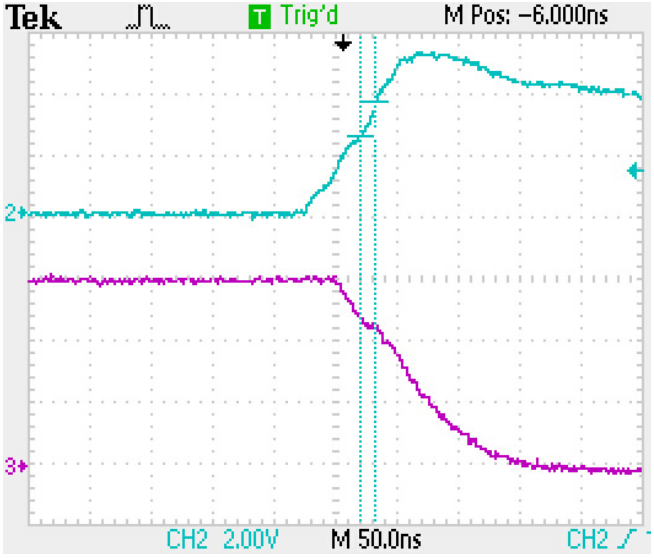

Fig. 7a. Miller plateau at the turn-on transient.

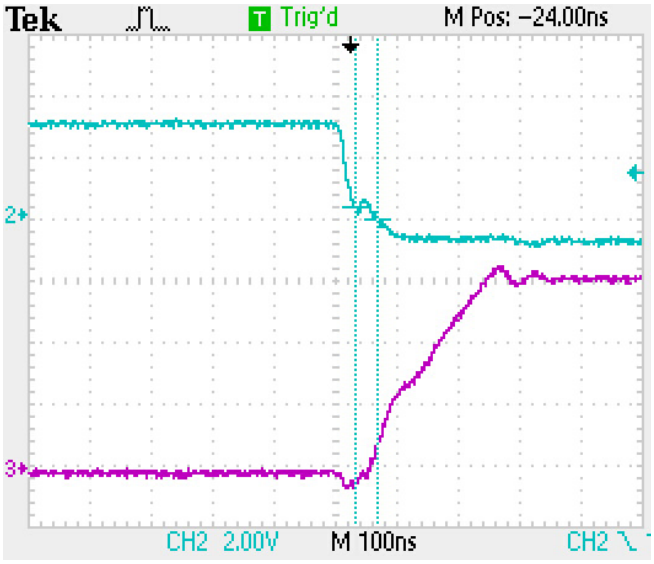

Fig. 7b. Miller plateau at the turn-off transient.

Conclusion

This paper investigates the gate drive characteristics of a SiC JFET and compares the differences with a MOSFET or IGBT. The influence of the gate drive on the switching characteristics of the device is investigated and the significant influence of the small input capacitance on the device switching speed is highlighted. The effect of the Miller capacitance was also investigated. Based on extensive practical measurements made on an actual SiC JFET switching at 50 kHz, a practical low cost driver circuit is proposed.